REMARKS

Claims 1-4 have been examined on their merits, and are all the claims pending in the application.

1. Claim 4 stands rejected under 35 U.S.C. § 101 as allegedly being non-statutory. Applicant herein amends claim 4 as suggested by the Patent Office. Applicant respectfully requests that the Patent Office reconsider and withdraw the § 101 rejection of claim 4.

2. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Blinne *et al.* (U.S. Patent No. 5,274,568) in view of Hasegawa (U.S. Patent No. 6,041,168) (hereinafter Hasegawa '168) and in further view of Hasegawa (U.S. Patent No. 5,528,511) (hereinafter Hasegawa '511). Applicant traverses the rejection of claims 1-4 for at least the reasons discussed below.

The Patent Office acknowledges that Blinne *et al.* fail to teach or suggest that, for at least one of a plurality of circuits, a library that comprises logical operation information. *See* April 25, 2005 Final Office Action, page 8. The Patent Office alleges that Hasegawa '168 supplies the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.*

The Patent Office acknowledges that the combination of Blinne *et al.* and Hasegawa '168 fail to teach or suggest logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of a plurality of circuits. The Patent Office further acknowledges that the combination of Blinne *et al.* and Hasegawa '168 fails to teach or suggest that the delay information is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output

terminals as represented by the logical operation information for the circuit. *See* April 25, 2005 Final Office Action, pages 8-9. The Patent Office alleges that Hasegawa '511 supplies the necessary disclosure to overcome the acknowledged deficiencies of the combination of Blinne *et al.* and Hasegawa '168.

Hasegawa '511 discloses, *inter alia*, a delay time verification methodology that provides propagation delay times even when the rising edge or the falling edge of a signal is meaningless. *See* col. 2, lines 63-65 of Hasegawa '511. The method disclosed by Hasegawa '511 uses nodes and arcs in a fashion similar to Hasegawa '168. *See, e.g.*, col. 5, lines 16-23 of Hasegawa '511.

With respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit, where the analysis library stores delay time information based on correspondence between the input terminal logical state transitions and the output terminal logical state transitions, and the delay information is selected based upon certain input/output terminal signal transitions. The combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not use input terminal logical state transitions, output terminal logical state transitions and delay information in the same manner as the present invention.

In the present invention, delay times are based upon the current logical state of a logic circuit, and the types of state transitions that are present on the input and output terminals of the logic circuit. A rising edge signal might have two different propagation delay times, based on the logical state of the circuit and the logical states of the other input signals.

Turning to the applied prior art, Blinne *et al.* are concerned with the propagation time of a rising or falling edge through a logic cell. *See* col. 1, lines 45-48 of Blinne *et al.* Blinne *et al.* do

not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Blinne *et al.* ignore the logic operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit. Inputs not being measured are fixed to a predetermined logic level while measuring the delay time of the remaining input. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.* In calculating the maximum delay time for the logic circuit, Blinne *et al.* uses the delay time of the input with the longest delay time. For example, this delay time is longer than what would be found in normal AND gate operation, because in that case the output falls as soon as the input with the shortest delay time falls.

Hasegawa '168 does not even teach or suggest signal transitions, but instead adds a series of maximum delay times together to determine a propagation delay. *See* col. 5, lines 23-34; Fig. 5 of Hasegawa '168.

While the circuit modeling technique disclosed by Hasegawa '511 uses rising and falling signals, Hasegawa '511 still rely upon maximum delay times, stored in the arcs between nodes, for propagation delay time calculations. *See* col. 6, lines 54-56 of Hasegawa '511. Hasegawa '511 does not teach or suggest determining delay time for "each signal path of said at least one circuit" based on the logical state transitions at the input and output terminals.

The Patent Office argues that Hasegawa '511 discloses the rise/fall transitions of the invention recited in claim 1. However, Hasegawa '511 also specifies that certain signal paths are "invalid" due to their rise/fall characteristics for certain signal paths, and that no signal path that contains an "invalid" identifier is used for delay calculations. *See, e.g.*, col. 3, lines 17-20; col. 4, lines 15-20; col. 6, lines 13-17 and Fig. 10 of Hasegawa '511.

The combining of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 with each other does not remove this fundamental deficiency which permeates each of the references. In the three references, the propagation delay time for a logic circuit is arrived at using maximum delay times, and there is no discussion of using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates. Moreover, the delay analysis in Hasegawa '511 is for a single-input, single-output circuit. The analysis disclosed for Figure 1 discards certain propagation paths, while claim 1 specifically recites that the propagation analysis is made for "each signal path of said at least one circuit." For example, Hasegawa '511 specifies that certain signal paths are "invalid" due to their rise/fall characteristics for certain signals, and that no signal path that contains an "invalid" identifier is used for delay calculations. *See, e.g.*, col. 3, lines 17-20; col. 4, lines 15-20; col. 6, lines 13-17 and Fig. 10 of Hasegawa '511. There is no teaching or suggestion in the combination of references that indicates that "invalid" signal paths are used in calculating delay time for logical state transitions. Thus, Hasegawa '511 cannot teach or suggest "making a delay analysis of each signal path of said at least one circuit" as recited in claim 1, since Hasegawa '511 clearly and unequivocally rejects making a delay analysis of those signal paths that are deemed to be "invalid" and not necessary for inclusion.

While Applicant admits that Hasegawa '511 does show determining delay time on the basis of an input signal's effect on a circuit's logical state, Hasegawa '511 does it in a completely different manner than the present invention. Hasegawa '511 discloses, *inter alia*, an invalidness specification means that specifies arcs (*i.e.*, signal paths) that have invalid data and arcs where either the rise or fall (but not both) of a signal is valid. *See, e.g.*, col 3, lines 17-20 of Hasegawa '511. Therefore, if a signal path has been declared to be invalid, or valid only for one of rise or

fall time, then Hasegawa '511 does not teach or suggest the recitations of claim 1 that recite that delay information is available for each signal path of the at least one circuit, and that input signal transitions for causing both low-to-high and high-to-low output terminal state transitions are to be considered. In contrast, the present invention recited in claim 1 uses delay time information for all signal paths of a particular circuit. Applicant submits that the Patent Office is failing to appreciate the distinction between Hasegawa '511, which avoids evaluating invalid signal paths, and the evaluation of all signal paths, as recited in claim 1. The fact that the present invention recited in claim 1 does not ultimately use timing information from certain signal paths should not be confused with the declaration of a signal path being invalid, as disclosed in Hasegawa '511.

In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest that a delay time is selected from delay time information according to input terminal and output terminal logical state transitions, as recited in claim 1. The Patent Office acknowledges that Blinne *et al.* fail to teach or suggest this feature of the present invention.[1] The Patent Office alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.* As discussed above, Hasegawa '511 does not teach or suggest determining delay time based on the current logical state of a circuit and the logical state transitions at the input and output terminals. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not use all the types of logical state transitions present

[1] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

between the input and output terminals of all paths in a logic circuit when selecting a delay time for a particular signal propagation path through the logic circuit.

Thus, Applicant submits that the Patent Office cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 1, as required by *In re Vaeck.*

Applicant submits that one of skill in the art would not be motivated to combine the three references. Although the Patent Office provides a generalized motivation analysis with respect to a delay analysis method, none of the references teaches or suggests providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input and output terminals as represented by stored logical operation information. As discussed above, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teaches or suggests that a delay time is selected from delay time information for each circuit path according to the type of logical state transitions present at both the input and output terminals of a circuit, as recited in claim 1. Since none of the references teaches or suggests these features of claim 1, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant submits that the Patent Office cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claim 1, as required by *In re Dembiczak* and *In re Zurko.*

Based on the foregoing reasons, Applicant submits that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest all of the claimed elements as arranged in claim 1. Thus, Applicant submits that claim 1 is in condition for allowance.

Applicant respectfully requests that the Patent Office reconsider and withdraw the § 103(a) rejection of claim 1.

With respect to claim 2, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay time information for a circuit that is based upon the type of logical state transitions present at the circuit's input and output terminals as represented by stored logical operation information and the delay information is selected based upon certain input/output terminal signal transitions. As discussed above with respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not use the type of logical state transitions at both the input and output terminals of a circuit in the same manner as the present invention. In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time for each signal path between an input terminal and an output terminal of a logic circuit from stored delay time information according to the type of logical state transitions for the input and output terminals.

As discussed above with respect to claim 1, Hasegawa '511 specifies that certain signal paths are "invalid" due to their rise/fall characteristics for certain signals, and that no signal path that contains an "invalid" identifier is used for delay calculations. *See, e.g.*, col. 3, lines 17-20; col. 4, lines 15-20; col. 6, lines 13-17 and Fig. 10 of Hasegawa '511. The Patent Office acknowledges that Blinne *et al.* fail to teach or suggest this feature of the present invention.[2]

The Patent Office alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.* As discussed above with respect to

[2] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

claim 1, Hasegawa '511 does not teach or suggest determining delay time for each signal path based on the type of logical state transitions present at both the input and output terminals of a logic circuit. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not use the type of logical state transitions for each circuit path between the input and output terminals when selecting a delay time for a particular signal propagation path through the logic circuit. As discussed above with respect to claim 1, the Patent Office does not appear to appreciate the distinction between not using a signal path in a timing analysis because it is "invalid" (Hasegawa '511) and evaluating a signal path but ultimately not using that evaluation in the timing analysis, as recited in claim 2. Thus, Applicant submits that the Patent Office cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Vaeck*.

Applicant submits that one of skill in the art would not be motivated to combine the three references. None of the references teaches or suggests providing delay information for a circuit that is based upon the type of logical state transitions for the input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time for each signal path between an input terminal and an output terminal of a logic circuit from stored delay time information according to the type of logical

state transition present at the input and output terminals and the delay information is selected based upon certain input/output terminal signal transitions, as recited in claim 2. Since none of the references teaches or suggests these features of claim 2, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant submits that the Patent Office cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicant submits that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest all of the claimed elements as arranged in claim 2. Thus, Applicant submits that claim 2 is in condition for allowance. Applicant respectfully requests that the Patent Office reconsider and withdraw the § 103(a) rejection of claim 2.

With respect to claims 3 and 4, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest referencing a delay analysis library comprising delay information for a circuit that is based upon the type of logical state transitions for each circuit path between the input and output terminals as represented by stored logical operation information and the delay information is selected based upon certain input/output terminal signal transitions. As discussed above with respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not reference a delay analysis library comprising the types of logical state transitions at input and output terminals that correspond to delay times in the same manner as the present invention. In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time for each circuit path based on the type of logical state transitions present at the input and output terminals of a logical circuit, as recited in claims 3 and 4.

The Patent Office acknowledges that Blinne *et al.* fail to teach or suggest at least this feature of the present invention.[3] *See* April 25, 2005 Final Office Action, page 10. The Patent Office alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.*

As discussed above with respect to claim 1, Hasegawa '511 does not teach or suggest determining delay time of each circuit path based on the type of logical state transitions present at the input and output terminals of a logical circuit. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not use the logical state transitions present at both the input and output terminals when selecting a delay time for a particular signal propagation path through the logic circuit. Also, as discussed above with respect to claim 1, Hasegawa '511 specifies that certain paths are "invalid" due to their rise/fall characteristics for certain signals, and that no signal path that contains an "invalid" identifier is used for delay calculations. *See, e.g.*, col. 3, lines 17-20; col. 4, lines 15-20; col. 6, lines 13-17 and Fig. 10 of Hasegawa '511. As discussed above with respect to claim 1, the Patent Office does not appear to appreciate the distinction between not using a signal path in a timing analysis because it is "invalid" (Hasegawa '511) and evaluating a signal path but ultimately not using that evaluation in the timing analysis, as recited in claims 3 and 4. Thus, Applicant submits that the Patent Office cannot fulfill the "all

[3] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

limitations" prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Vaeck.*

Applicant submits that one of skill in the art would not be motivated to combine the three references. None of the references teaches or suggests providing delay information for each path of a circuit that is based upon the type of logical state transitions present at the circuit's input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time for each signal path from delay time information according to input and output terminal logical state transitions of a circuit and the delay information is selected based upon certain input/output terminal signal transitions, as recited in claims 3 and 4. Since none of the references teaches or suggests these features of claims 3 and 4, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant submits that the Patent Office cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Dembiczak* and *In re Zurko.*

Based on the foregoing reasons, Applicant submits that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest all of the claimed elements as arranged in claims 3 and 4. Thus, Applicant submits that claims 3 and 4 are in condition for allowance. Applicant respectfully requests that the Patent Office withdraw the § 103(a) rejection of claims 3 and 4.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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